LABORATORY MANUAL

CPE101/SC101: Electronic Principles/Electronics 1
Electronics Lab (N4 B1C-17)

No. 5 Transistor Switching Circuits

SESSION 2005-2006
SEMESTER 1
COMPUTER ENGINEERING COURSE

SCHOOL OF COMPUTER ENGINEERING
NANYANG TECHNOLOGICAL UNIVERSITY

TRANSISTOR SWITCHING CIRCUITS

1. OBJECTIVE

To observe actual transistor switching characteristics and appreciate their operation in:

(i) several simple transistors circuits

(ii) TTL and CMOS logic IC which use the transistor to operate as an ON/OFF switch.

2. LABORATORY

Electronics Laboratory.

3. EQUIPMENT

3.1 Instrument

DC Power supply
Dual Trace Oscilloscope
Digital Multimeter
Function Generator
Project breadboard

3.2 Components

Description		*Qty*	*S$ / unit*	*Remarks*
Transistor	2N2222	1	0.08	NPN
Digital IC	74LS04	1	0.25	TTL Hex Inverters
Digital IC	MC14001	1	0.25	CMOS NOR Gates
Resistor	1 kΩ	1	0.01	
Resistor	6.8 kΩ	2	0.01	

(*Note: you will need a sheet of linear graph paper for graph plotting purpose.)

4. INTRODUCTION

Operation of the transistor in the switching mode is fundamental to the implementation of digital electronic circuits and systems.

In this experiment we shall first examine the switching performance of transistors by building and observing the operation of simple logic gates (the 2N2222 transistor will again be used to build simple transistor circuits for analysis). Subsequently the switching performance of standard TTL and CMOS gates will also be studied and examined in detail.

4.1 The Simple Inverter

The inverter is the simplest transistor switch and is shown in figure 1.

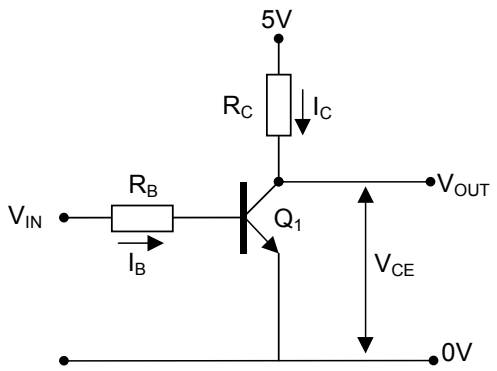

Figure 1. The transistor in simple inverter configuration.

R_B is selected so that when $V_{IN} = V_{CC}$ the transistor is *overdriven* sufficiently to ensure that it is saturated, that is, $V_{OUT} = V_{CE_{sat}}$ (~0V) and $I_C = V_{CC}/R_C$. The resulting waveforms at V_{IN} and V_{OUT} are of the form shown in figure 2 where the output is the inverse of the input.

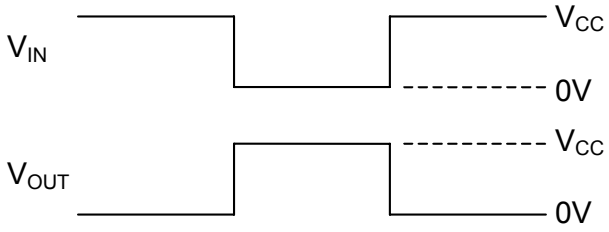

Figure 2. Idealised response of the single transistor inverter.

In practice, the transistor switch does not exhibit the ideal behaviour implied by the input and output waveforms shown in figure 2. Figure 3 shows a more realistic picture of a circuit like the inverter, illustrating the variation of collector current that will occur for a sharp-edged pulse at the input. In particular, note the various timing degradation. The scale of the drawings is just an approximation.

The time duration that is of interest for digital circuits are:

t_d - delay time during turn on;

t_r - 10%-90% rise time;

t_s - storage time during turn off;

t_f - 90%-10% fall time

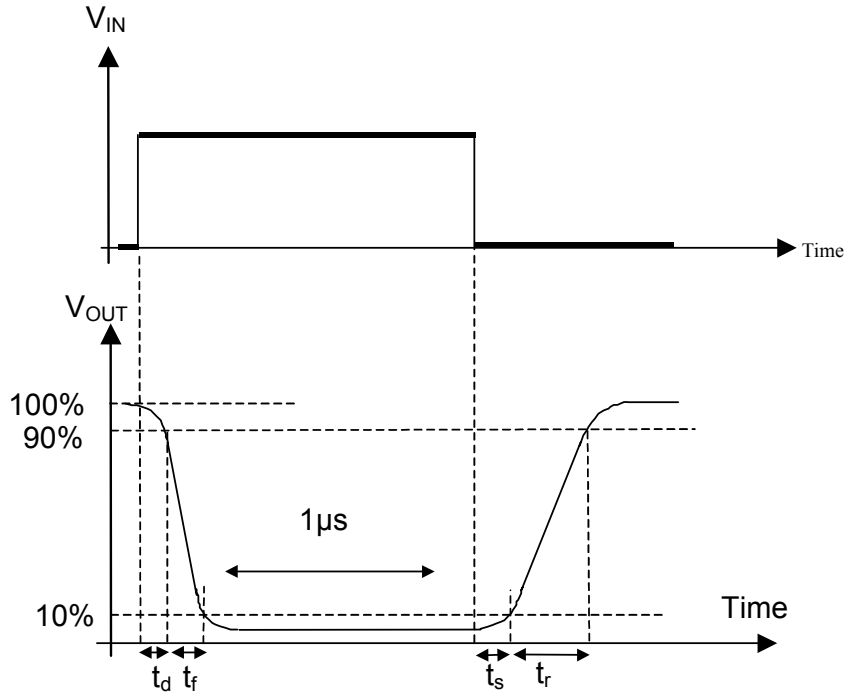

Figure 3. Output voltage response to sharp square wave base input for a transistor working as an inverting switch.

The time delays can be significant at high switching speeds, so the useful switching rate of the simple inverter is quite low. The causes of the degradation in speed are the various inter-electrode capacitances within the transistor, and 'charge storage' in the base region.

Q The rise-time of the current V_{OUT} is shown as significantly longer than its fall-time: this is not a mistake in the 'artwork' - what is the electrical explanation?

4.2 Two-Input Inverter (NOR Gate)

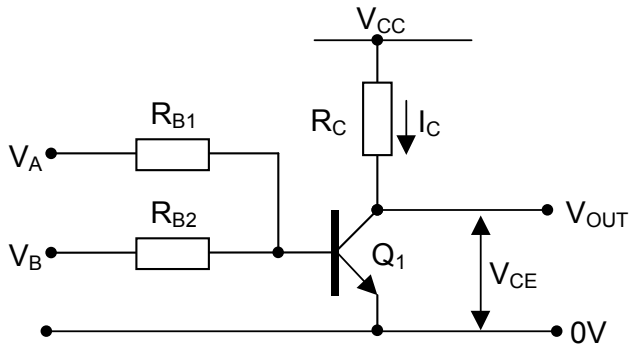

Figure 4. Simple inverter with two inputs.

If we assume positive logic where 5 V is logic '1' and 0 V is logic '0' then the circuit shown on figure 4 forms a two-input NOR gate. This is assumed that the resistor values have been chosen such that sufficient base current will flow to saturate the transistor Q_1 if *either* input V_A *or* input V_B is HIGH (or vice versa).

Interestingly, if we assume negative logic convention where +V is logic '0' and 0 V is logic '1' then the circuit of figure 4 forms a two-input NAND gate. In the remainder of this experiment we will assume the more usual positive logic convention.

4.3 A TTL Switch

The internal circuit of a TTL inverter is shown in figure 5. Compared to the single transistor inverter circuit of figure 1, we can see that the 'load' of the output transistor Q_4 is an emitter follower. The R_4, Q_3, D_1 and Q_4 configuration is known as a totem pole output stage. This enables faster switching of the output state of Q_4 from low to high. Q_2 operates as an intermediate amplifier which increases the input voltage for an output level transition from one to two diode voltages and provides complementary input currents to the totem pole output stage; Q_1 at the input is in reverse active mode and greatly improves the switching speed during a low-high output transition.

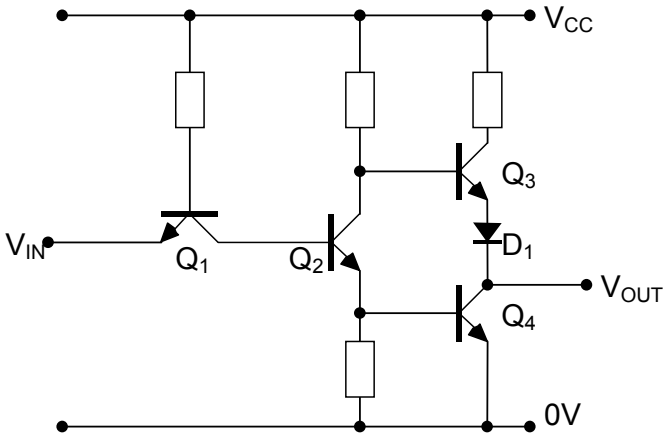

Figure 5. TTL inverter circuit.

5 EXPERIMENT

5.1. Dynamic Operation of the BJT Inverter

1. Construct the circuit shown in figure 6.
2. Apply a 500-Hz signal from the TTL output of the signal generator to V_1. Observe both the input V_1 and the output V_{OUT} on the oscilloscope and gradually increase the frequency from 500 Hz to 150 kHz, noting and recording the changes in V_{OUT}. Explain the rise time and fall time components observed.
3. To observe V_1 and V_{OUT} on the oscilloscope, should you use the 'ALT' or 'CHOPPED" mode? 'AC' or 'DC' coupling? Explain.

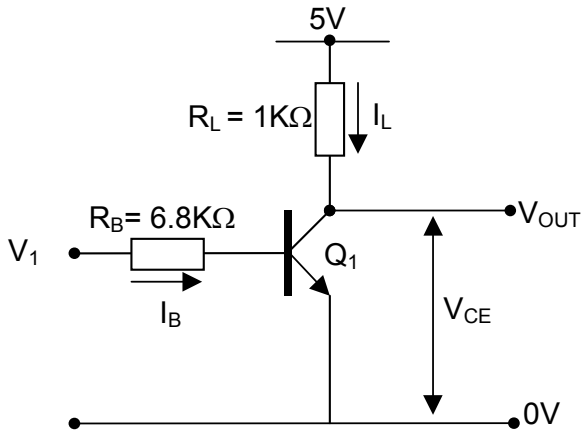

Figure 6. BJT inverter

5.2 A Simple NOR Gate and Observe its Operation

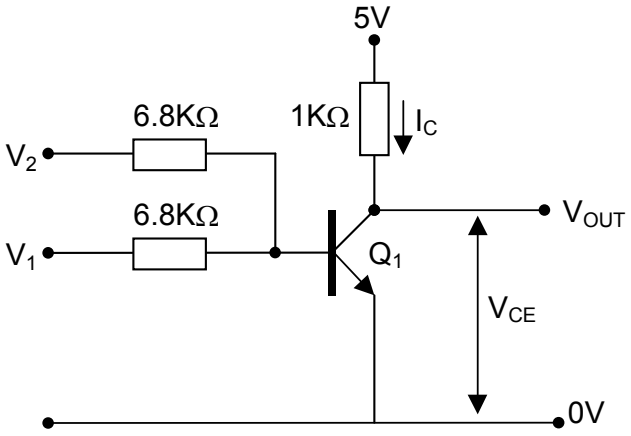

Figure 7. Two-input switch

1. Modify the circuit of figure 6 by including an additional input as shown in figure 7.
2. Apply a 500-Hz signal from the TTL output of the signal generator to V_1.
3. Set input V_2 to +5 V and observe the output V_{OUT}.
4. Now set input V_2 to 0 V and observes the output V_{OUT}.
5. Validate that the observed behaviour is as expected and comment on the effect if more inputs are used to implement a 3-, 4-, 5-, … input logic gate.

5.3. Dynamic operation of the TTL circuit

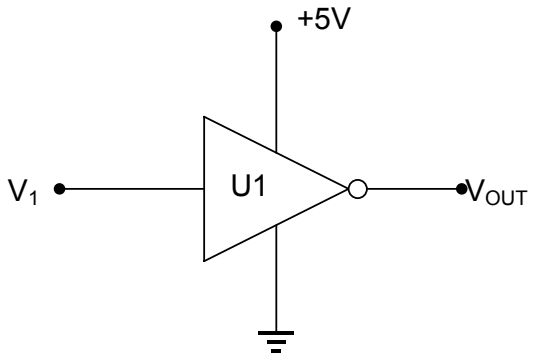

Figure 8. Single TTL Inverter

1. Construct the circuit shown in figure 8, using the 74LS04 logic gate IC.
2. Gradually increase the voltage V_1 from 0v to +5V, noting the point at which V_{OUT} changes rapidly for small changes in the input. Plot a graph of V_{OUT} against V_1. Compare this with the voltage transfer characteristics obtained with the single transistor inverter from the previous experiment. Estimate the noise margin of the IC from your results.
3. Apply a 500-Hz signal from the TTL output of the signal generator to V_1. Observe both the input V_1 and the output V_{OUT} on the oscilloscope and gradually increase the frequency from 500 Hz to 150 kHz, noting and recording the changes in V_{OUT}.
4. Compare this result with that obtained from 5.1 and validate that the switching speed and characteristic is as expected.

5.4. Examine the switching speed and performance of a TTL gate

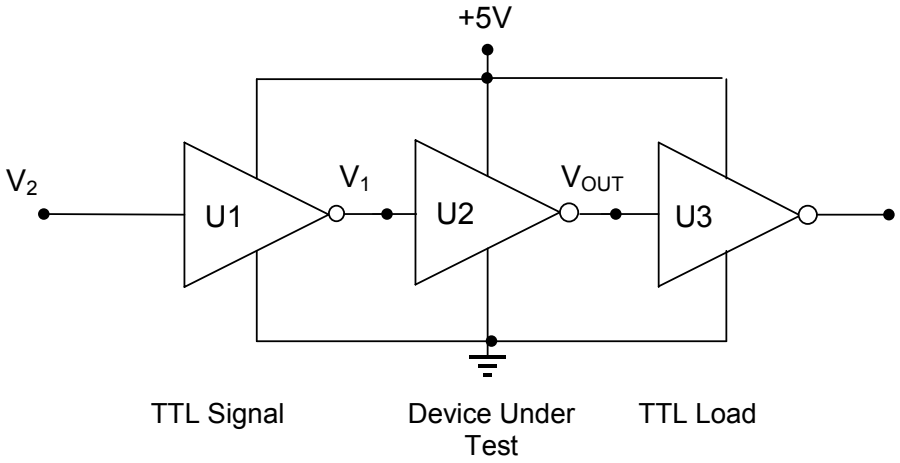

Figure 9. TTL gate

1. Connect three of the six inverters on the TTL 74LS04 device as shown in Figure 9 and apply a 1-KHz TTL square wave at V_2. The specifications and pin layout for the 74LS04 is given in the appendix. The first gate U1 is used to shape the waveform, ensuring that the gate under test, U2, is presented with a true TTL input at all frequencies used in this experiment and is not influenced unduly by the switching speed of the signal generator. The final gate, U3 is connected as a single standard TTL load for the gate under test.
2. Starting from 1 kHz, increase the frequency of the signal generator gradually to 2 MHz (you may need to change the oscilloscope mode to ALT at very high frequency) and compare the switching speed and delay between the input signal at V_1 and the output signal at V_{OUT}. In particular note the rise and fall times of the input to U2 at V_1 and its output at pin V_{OUT}.

5.5 DC Fan-out of the 74LS04

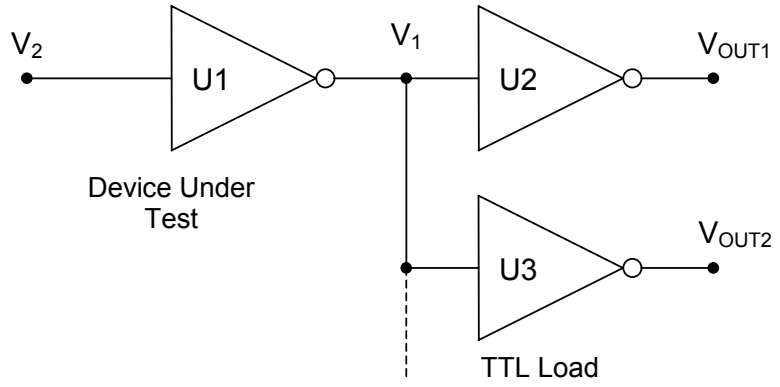

Figure 10. Fan-out

1. Reconnect the logic gates such that one gate is used to drive two others as shown in figure 10. Remember to connect V_{CC} and GND.
2. Apply a logic low to the input V_2 and measure the output voltage V_{OUT1}, V_{OUT2} of the driven gates. Check whether the output states are as expected and measure the value at V_1.
3. Increase the number of driven gates; record the value of V_1 for each increment and confirm the logic levels at the output of the driven gates. Comment on the DC fan-out performance of the 74LS04 logic device.

5.6 Examine the switching speed and performance of a CMOS gate

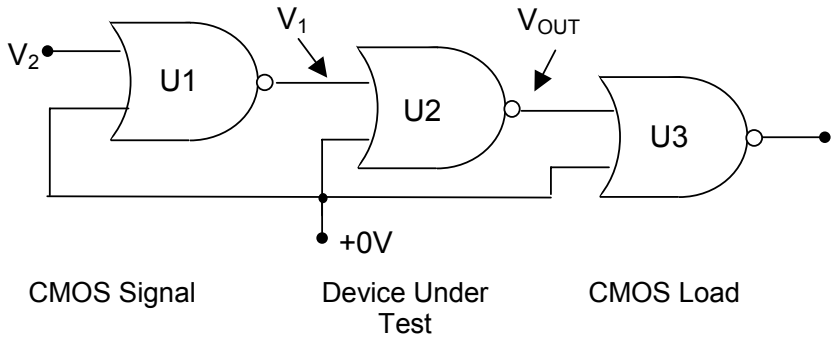

Figure 11. CMOS NAND gate.

1. Connect three of the four NOR gates of the CMOS MC14001 device as shown in Figure 11 and apply a 1-KHz TTL square wave at V_2. The specifications and pin layout for the MC14001 is given in the appendix. As the NOR gate has two inputs we will tie the other input to logic low. Why?
2. Starting from 1 kHz, increase the frequency of the signal generator gradually to 2 MHz and compare the switching speed and delay between the input signal at V_1 and the output signal at V_{OUT}. In particular note the rise and fall times of the input to U2 at V_1 and its output at pin V_{OUT}.
3. Compare the results with those in 5.4.

5.7 DC Fan-out of the CMOS MC14001 (*Note: This part is optional)

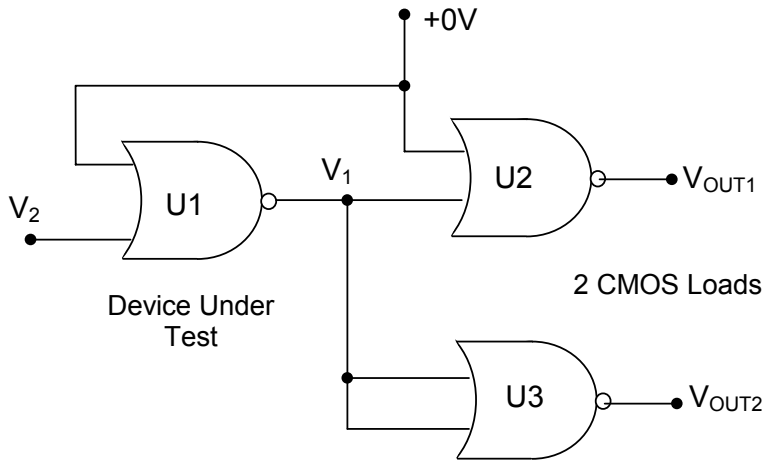

Figure 12. CMOS Fan-out

1. Reconnect the CMOS NOR gates such that one gate is used to drive two others as shown in figure 10.
2. Apply a logic low to the input V_2 and measure the output voltage of the driven gates. Check whether the output states are as expected and measure the value of V_1.
3. Increase the number of driven gates. Note that when both inputs are connected to the output of the previous gate, we have a load of two. Record the value of V_1 for each increment and confirm the logic levels at the output of the driven gates. Comment on the DC fan-out performance of the CMOS logic device.

5. REFERENCES

Data sheets for 74LSxx and MC140xx TTL and CMOS logic gates.