CPE101 Laboratory Experiment 5

Transistor Switching Circuits

Formal Report

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TRANSISTOR SWITCHING CIRCUITS

1. OBJECTIVE

To observe actual transistor switching characteristics and appreciate their operation in:

(i) several simple transistors circuits

(ii) TTL and CMOS logic IC which use the transistor to operate as an ON/OFF switch.

2. LABORATORY

Electronics Laboratory

3. EQUIPMENT

3.1 Instrument

- DC Power supply
- Dual Trace Oscilloscope
- Digital Multi-meter
- Function Generator
- Project breadboard

3.2 Components

Description		*Quantity*	*S$ / unit*	*Remarks*
Transistor	2N2222	1	0.08	NPN
Digital IC	74LS04	1	0.25	TTL Hex Inverters
Digital IC	MC14001	1	0.25	CMOS NOR Gates
Resistor	1 KΩ	1	0.01	
Resistor	6.8 KΩ	2	0.01	

4. INTRODUCTION

The **transistor** is a solid state semiconductor device which can be used for amplification, switching, voltage stabilization, signal modulation and many other functions.

There are many types of transistors for different purposes. However, in this experiment, we will use 2N2222 transistor to build the simple logic gates. Next we will observe the operation of standard TTL and CMOS.

4.1 The Simple Inverter

The simplest inverter is made of a transistor Q_1, resistors R_B and R_C, V_{CC} and V_{IN}. If R_B is chosen to make Q_1 saturated while $V_{IN} = V_{CC}$, then $V_{CE(sat)}$ tends to zero volt. Therefore, by KVL we have $V_{CC} - I_C.R_C - V_{CE(sat)} = 0$.
But $V_{CE(sat)}$ tends to 0 when Q_1 is saturated, hence $V_{CC} - I_C.R_C = 0$ or $I_{C(sat)} = V_{CC}/R_C$

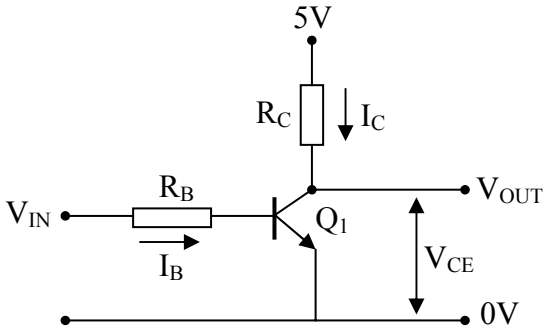


Figure 1. The simplest inverter

For the sake of illustration, suppose that inverter performs in ideal manner. It means that there is no leakage of energy and power in resistors and transistor. Thus, the inverter can be used as switch shown in figure 2.

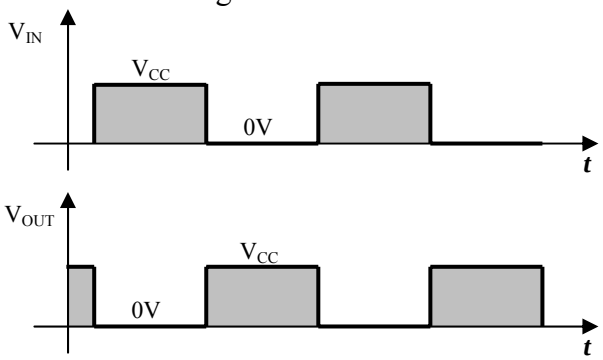
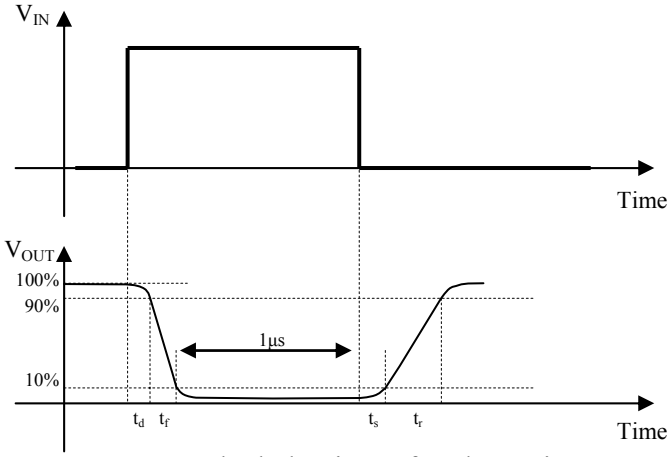


Figure 2. Ideal logic inverter

The figure 2 shows what an ideal inverter does; however, in real life, the transistor does not perform ideally shown in figure 2.

The actual voltage of V_{OUT} does not change immediately between cut-off and saturation offsets, but it gradually changes after the certain time delays. The figure 3 shows how the real transistor behaves.



t_d : delay time during turn on
t_r : 10%-90% rise time
t_s : storage time during turn off
t_f : 90%-10% fall time

Figure 3. The behaviors of real transistor

Question: The rise-time of the current V_{OUT} is shown as significantly longer than its fall-time: this is not a mistake in the 'artwork'- what is the electrical explanation?

Answer : We see that when the input V_{IN} is in the logic HIGH, V_{IN} is large enough to draw larger charging current I_B which causes the BJT to saturate more quickly and decreases the fall-time of V_{OUT}. There also will be more excess minority carrier charge stored in the base region due to internal capacitive effects after the BJT is turned on.

While V_1 is switched back to the logic LOW, the base current is reserved. As long as significant charges are still stored in the base region, the collector current will continue to exist. The removal of the excess charges can take a significant rise-time to make the V_{OUT} remaining in the steady state.

4.2 Two-Input Inverter (NOR Gate)

The simplest inverter may not be so useful in many purposes; hence the multi-input invert was introduced. For the sake of this illustration, we examine the Two-Input Inverter.

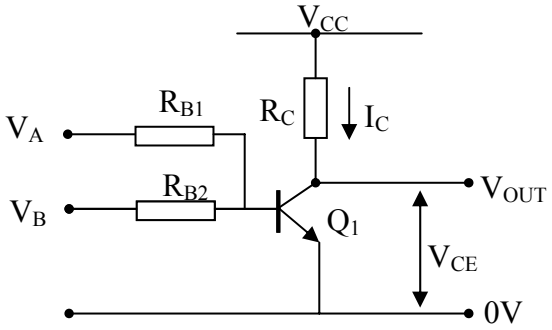


Figure 4. Two-Input Inverter

It is called two-input invert (NOR gate) if it has two input voltage sources and it behaves the characteristics of NOR gate. To clarify this, let us see the truth table:

A	B	A or B	Not (A or B)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Let '0' be the logic LOW of 0V and '1' be the logic HIGH of 5V.

- If V_A and V_B are in logic LOW, then the voltage at the base is zero and Q_1 is turned off; therefore $V_{OUT} = V_{CC}$ which is the logic HIGH
- If at least one of V_A and V_B is in the logic HIGH, and R_{B1} and R_{B2} are chosen to make the Q_1 saturated, V_{OUT} will result in the logic LOW

However, if we choose the inversed notations, i.e. 0V is logic HIGH and 5V is logic LOW, then the NOR gate becomes NAND gate.

4.3 A TTL Switch

TTL (Transistor-Transistor Logic) inverter is evolved from diode-transistor logic. The complete TTL gate circuit contains 3 parts: the Input stage, the Driver stage and the Output stage. In standard TTL, when the gate input state goes low, the input multi-emitter transistor operates in the normal active mode and supplies a large collector current to discharge the base of the phase splitter rapidly.

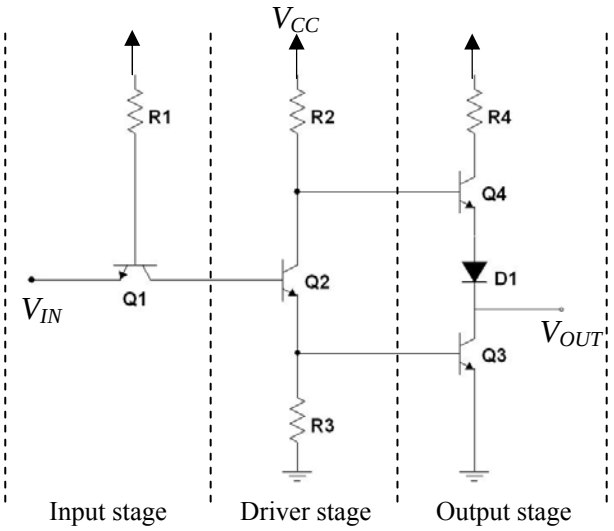


Figure 5. The complete TTL gate circuit with only one input terminal indicated

The totem-pole output stage consists of a common-emitter transistor, which can sink large load currents and thus rapidly discharge the load capacitance, and an emitter follower, which can source large load currents and thus rapidly charge the load capacitance.

5. EXPERIMENT

5.1 Dynamic Operation of the BJT inverter

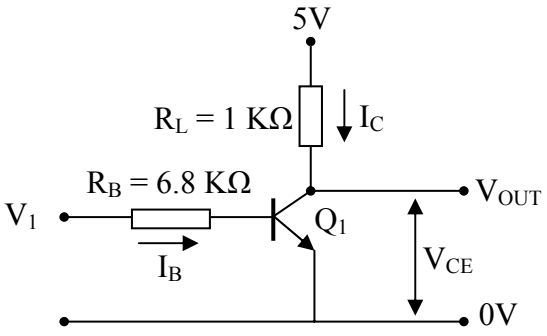


Figure 6. BJT inverter

When we apply a 500-Hz signal from the TTL output of the signal generator to V_1, the switching speed of the logic gate could be considered as a good switch. However, if we apply a high input frequency to V_1, there is the rise-time and fall-time phenomena happen. The rise-time takes longer period than the fall-time due to the internal capacitance effects explained in 4.1.

The higher frequency we apply to input voltage, the longer storage-time it takes. This happens because the switching speed of the input voltage is too fast for the internal capacitor at the base to charge and discharge. The figure below shows the wave forms at different frequencies.

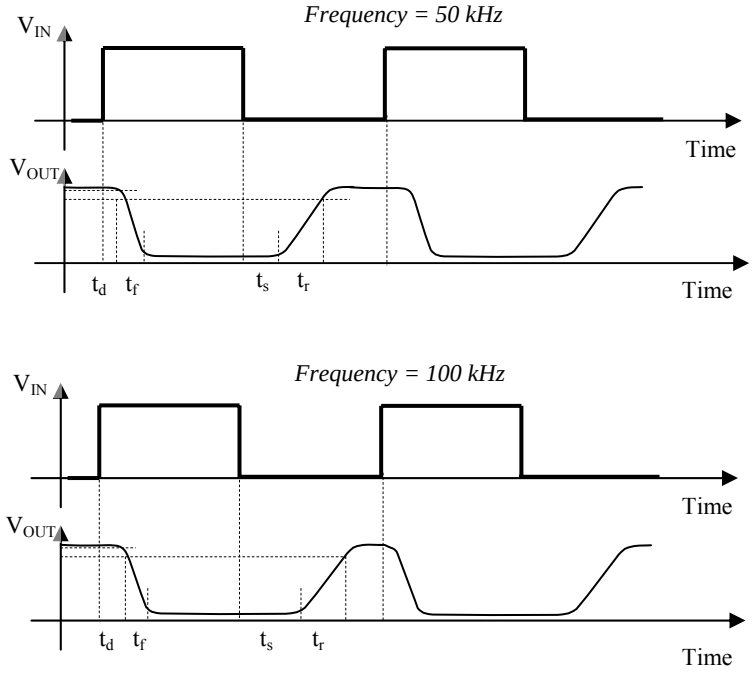


Figure 7. Wave forms of BJT inverter at different frequencies

To observe V_1 and V_{OUT} on the oscilloscope, we should use "DC" coupling because when we use "AC" coupling, the graph will take the ground line to be the average of the input and output; hence it would be so confused while the function generator provides maximum 4.0-5.0 V range of TTL signal to input and the V_{CC} is 5 V. Besides this, the purpose to use "DC" coupling is that what we want to observe is the signal of logic LOW (around 0 V) and logic HIGH (around 5 V) which does not relate to the negative voltage.

- At low frequency, we can use either "ALT" or "CHOP" mode.
- At high frequency, we use "ALT" mode.

Note: when we use "ALT" mode, we have to adjust the triggering setting to CH1 or CH2 in order to have the synchronized time line.

5.2 A Simple NOR Gate and Observer its Operation

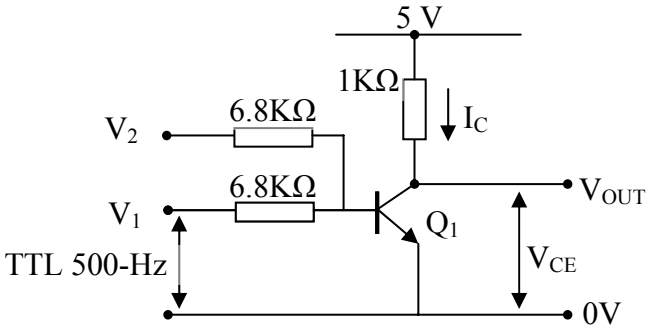


Figure 8. Two-Input Inverter

This circuit is the two-input inverter which can be used as a switch. It behaves as a NOR gate at which V_{OUT} is at logic HIGH when both of the inputs are at logic LOW and V_{OUT} is at logic LOW if at least one of the both inputs is at logic HIGH.

When we apply a 500-Hz signal from the TTL output of the signal generator to V_1, the signal at V_1 has the characteristics like the signal of pulse voltage source which swaps the value of 0 V and 5 V.

* If the V_2 is set to +5 V, then V_B is large enough to turn Q_1 into saturation mode and V_{OUT} is always at logic LOW

* If the V_2 is set to 0 V, the V_{OUT} will behave like the output voltage of single input TTL circuit. The difference between them is that the storage time of two input switch will be shorter than the storage time of the single input switch because of the parallel resistive effects.

* If more inputs are used to implement a 3-, 4-, 5-, … input logic gate, the V_{OUT} will become more accurate (V_{OUT} tends to ideal switch). However, if there are two many inputs which are set to 0 V, V_1 may not be strong enough to draw the currents into each additional input and Q_1 is unable to turn into saturation mode.

5.3 Dynamic operation of the TTL circuit

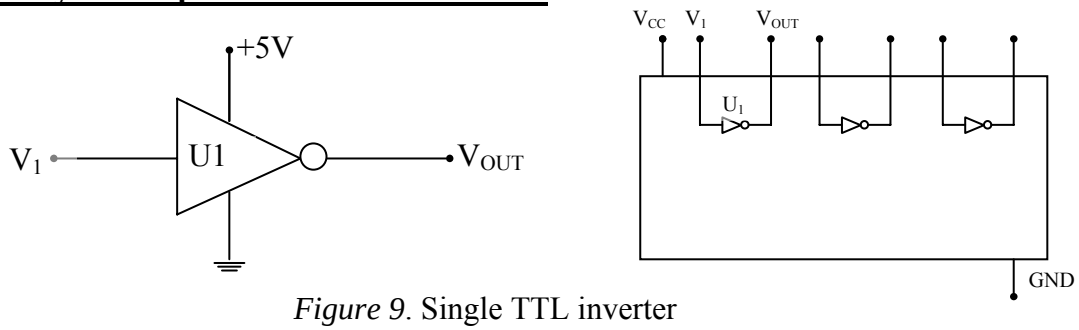


Figure 9. Single TTL inverter

The figure above is a single TTL inverter built by IC. To see how TTL inverter behaves, let us see the results of the experiment:

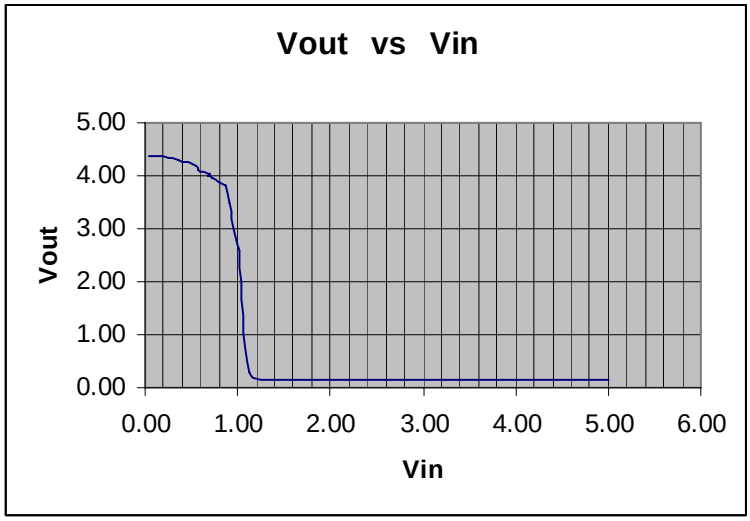


Figure 10. TTL circuit

Vin (V)	Vout (V)
0.05	4.37
0.13	4.36
0.26	4.34
0.35	4.29
0.55	4.20
0.58	4.11
0.69	4.05
0.67	4.00
0.72	3.97
0.86	3.81
0.92	3.48
0.98	2.84
1.02	2.44
1.13	0.28
1.41	0.15
1.91	0.15
2.60	0.15
4.00	0.15
5.00	0.15

From this experiment, we see that the IC provides the better characteristics of switching speed rather than single transistor from the previous experiment.

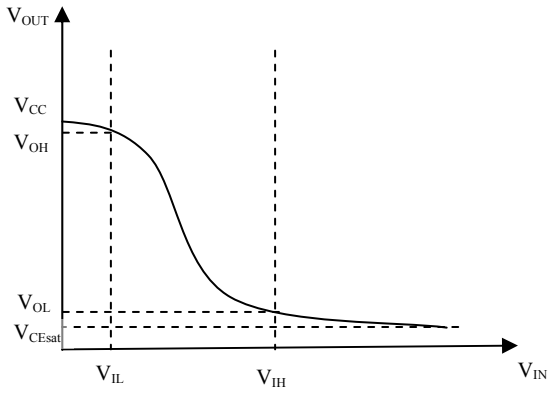


Figure 11. Single transistor in the previous experiment

Estimation of the noise margin of the IC:

From the graph, we have $V_{IL} = 0.4$ V, $V_{IH} = 1.2$ V, $V_{OL} = 0.2$ V, and $V_{OH} = 4.1$ V
Therefore, $NM_L = V_{IL} - V_{OL} = 0.4 - 0.2 = 0.2$ V
$NM_H = V_{OH} - V_{IH} = 4.1 - 1.2 = 2.9$ V

When we apply 500-Hz signal from the TTL output of the signal generator to V_1, the single TTL inverter could be considered as a perfect switch. Even though we apply the

high frequency 150-KHz, the output signal is still much better than that of single transistor.

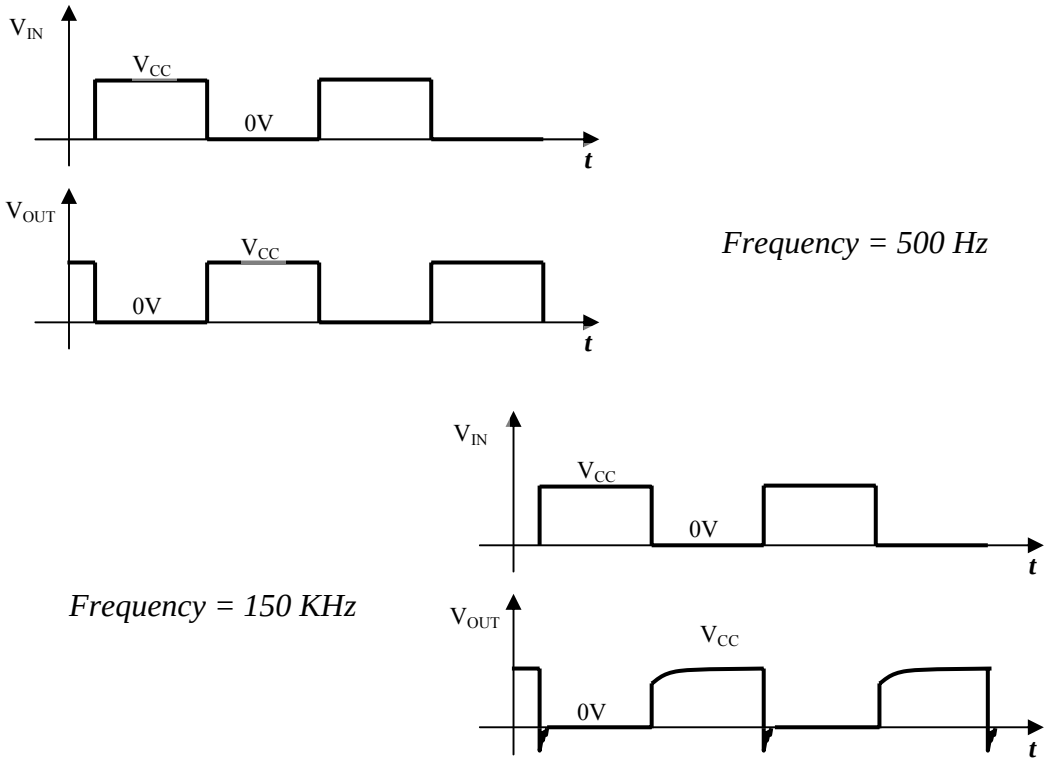


Figure 12. Wave forms of TTL circuit at different frequencies

This result shows that the switching speed of TTL circuit at low or high frequency is much better than the switching speed of BJT inverter elaborated in 5.1.

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