5.4 Examine the switching speed and performance of a TTL gate

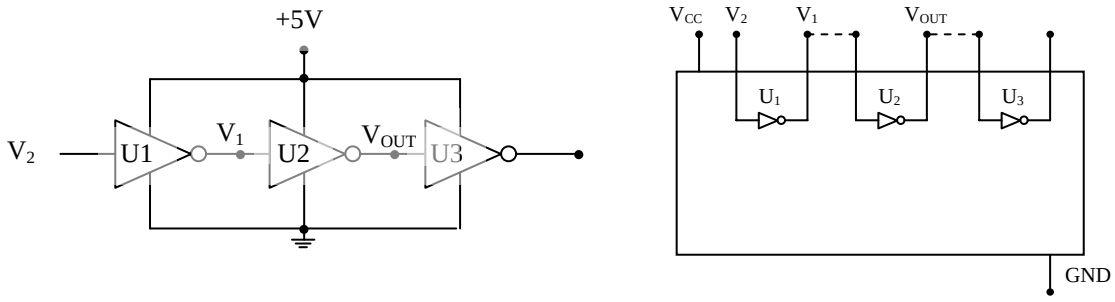


Figure 13. TTL gate

The above figure is the TTL gate; the output of U_1 is the input of U_2 at V_1. Thus, the switching speed of V_1 and V_{OUT} will not be affected by the V_2. When we apply a low frequency at V_2, U_2 behaves as a perfect square wave switch. Nevertheless, the rise-time and fall-time will happen once the high frequency (say 2 MHz) is applied to V_2. Interestingly, the rise-time and fall-time at V_1 and V_{OUT} are more or less the same. This phenomenon can be described by the graph below:

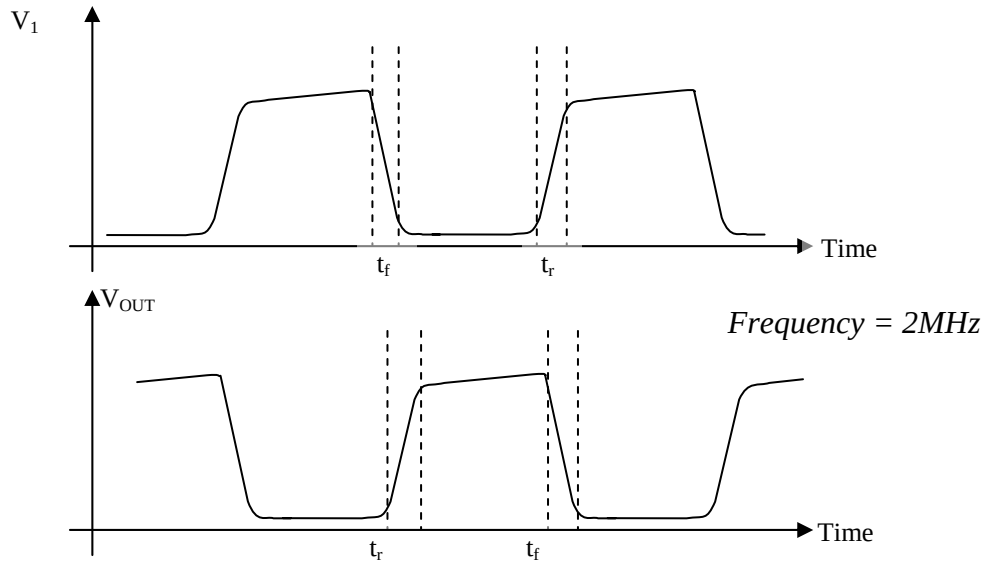


Figure 14. The responding signals of U_2 at V_1 and V_{OUT}

5.5 DC Fan-out of the 74LS04

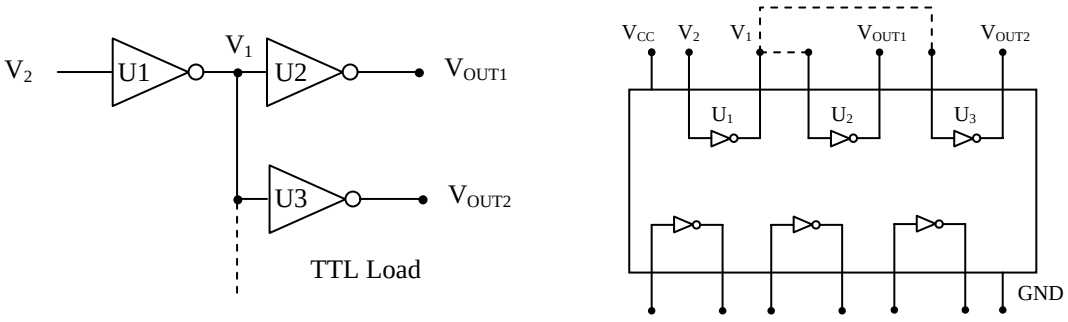


Figure 15. Fan-out

These logic gates are designed to make U_1 to drive other loads. It is useful when we want to have the multiple switches.

When we apply the logic LOW to the input V_2, then the output voltages V_{OUT1} and V_{OUT2} of the driven gates will be at logic LOW like V_2.

Explanation:
* When V_2 is at logic LOW, the output of U_1, V_1 is at logic HIGH. Therefore, the outputs of U_2 and U_3 are logic LOW.

If the number of the driven gates is increased, the value of V_1 will slightly increase due to the parallel resistance effects of the TTL loads, and the logic levels of the driven gates are at logic LOW like V_2. The good point of this circuit is that the more loads are connected to V_1, the better switching speed it is.

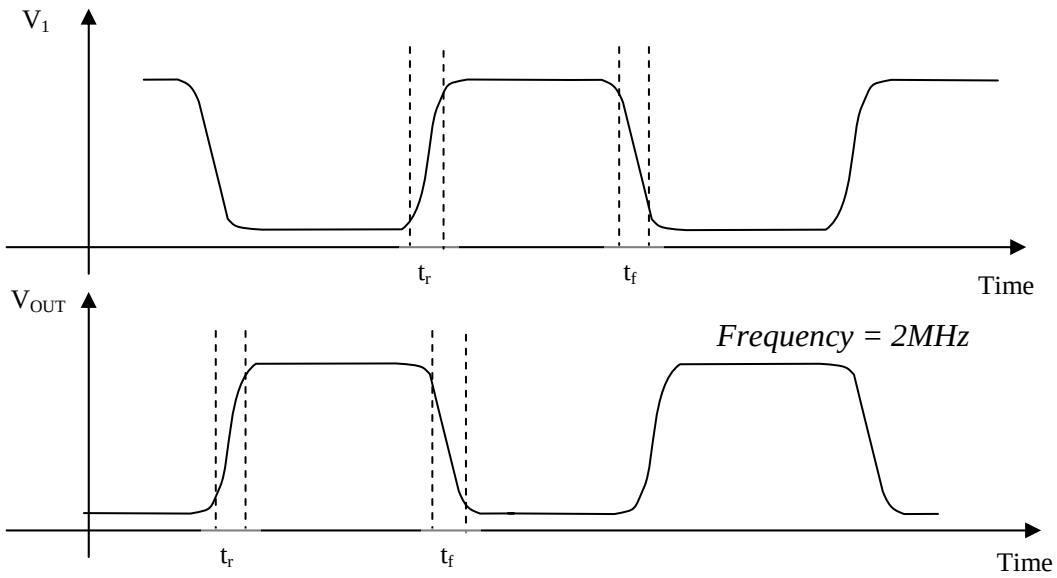


Figure 16. Signals of fan out

5.6 Examine the switching speed and performance of a CMOS gate

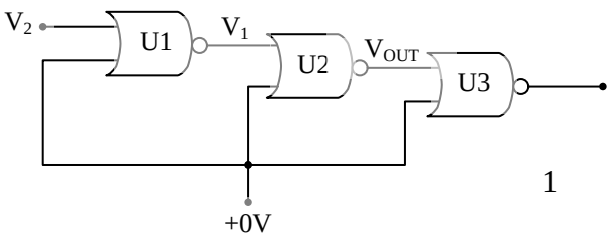
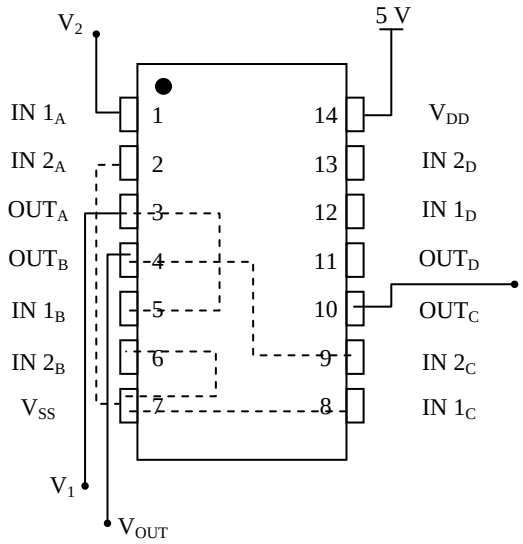


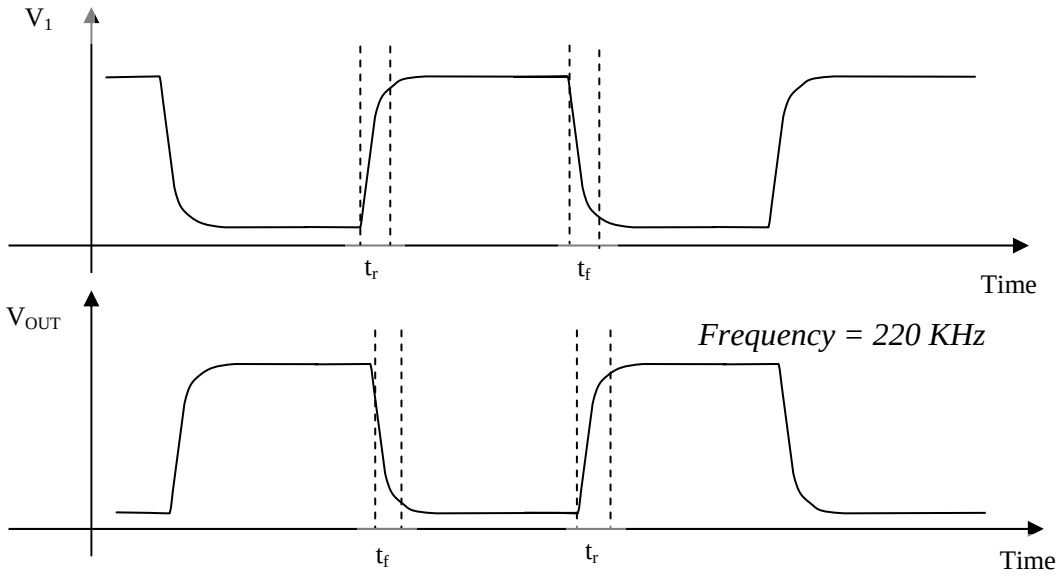
Figure 17. CMOS NAND gate

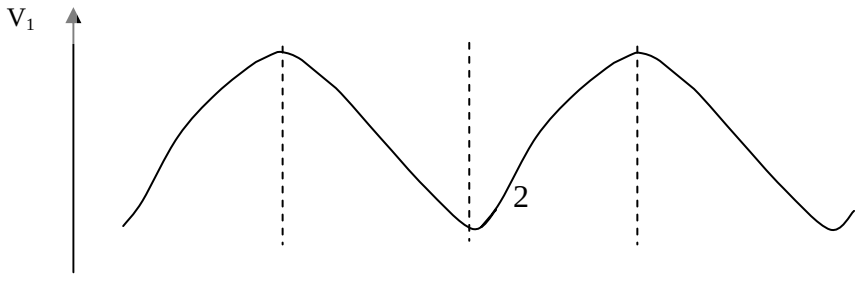
The right diagram shows how to connect the CMOS which is equivalent to the above circuit.

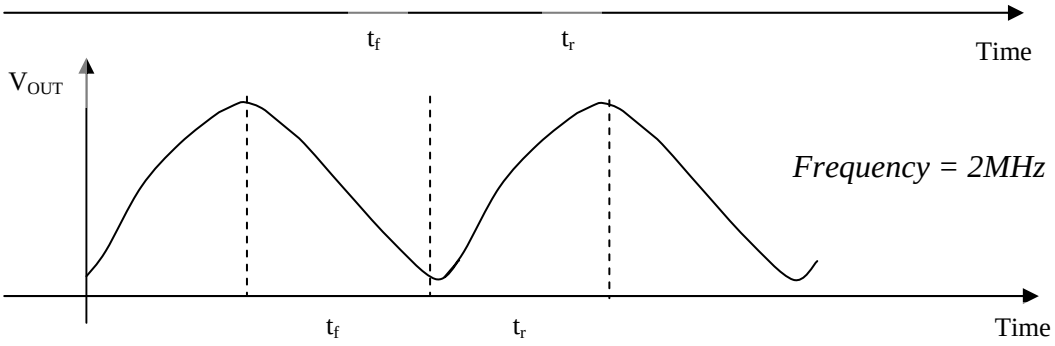


There are two inputs in NOR gate, and we have to connect one of the input to logic LOW. The reason behind this is that it is a NOR gate; if one of the input is connected to the logic HIGH, then the output of the gate will be always at logic LOW no matter what another input is at logic HIGH or logic LOW. This is the characteristics of the NOR gate. Therefore, if we want to make the switch useful, we have to connect one of the inputs to the logic LOW.

When we apply a low frequency at V_2, the device under test, U_2, behaves as a perfect square wave switch. However, if we apply the high frequency at V_2, rise-time and fall-time phenomena will dominate the switching speed.







The rise time and fall time dominate the switching speed when V_2 is at high frequency. It clearly shows that CMOS gate does not behave as a good switch as TTL gate at high frequency in 5.4.

6. CONCLUSION

Summary of the experiment:

- The simple inverter made by BJT has an important role of switch the logic gate. When input is at logic LOW, then output is at logic HIGH and vice versa. However, the switch does not behave perfectly as a square wave form; the output has the delay time, fall time, storage time and rise time. If the input is supplied with high frequency voltage, the output takes longer time for storage-time and rise-time. Therefore, the output curve may damage the square wave form.

- Single input BJT inverter may be so useful when there are multiple inputs; hence, the multi-input switch is introduced. The inputs are connected as parallel circuit at base of BJT. The good point of this switch is that we can control switch by many inputs, and the switching speed improved as the more inputs are connected.

- Since the single transistor does not perform well in switching speed, Integrated Circuit is introduced to improve the performance of switching speed. The switching speed of the TTL circuit is much better than that of the single transistor.

- When the inverts in IC are connected in series, the device under the test will not be affected by the input signal generator. In this sense, it means that rise-time and fall-time of the input signal are more or less the same as output signal.

- Even though TTL circuit is useful in many aspects, TTL device is far from ideal because it is considerable power consumption, non-zero input/output steady state current and low and unequal noise margin. This is why CMOS is invented.

- Even though CMOS device exhibits better performance compared to the TTL in the area of static power dissipation and noise margin, the drawback of CMOS is that TTL has advantages of CMOS in terms of the switching speed at high frequency.

In this experiment, we have really learnt many things which are very useful to continue to understand the higher level of electronics because it provides the very fundamental of the characteristics of the circuit switches and logic gates.

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